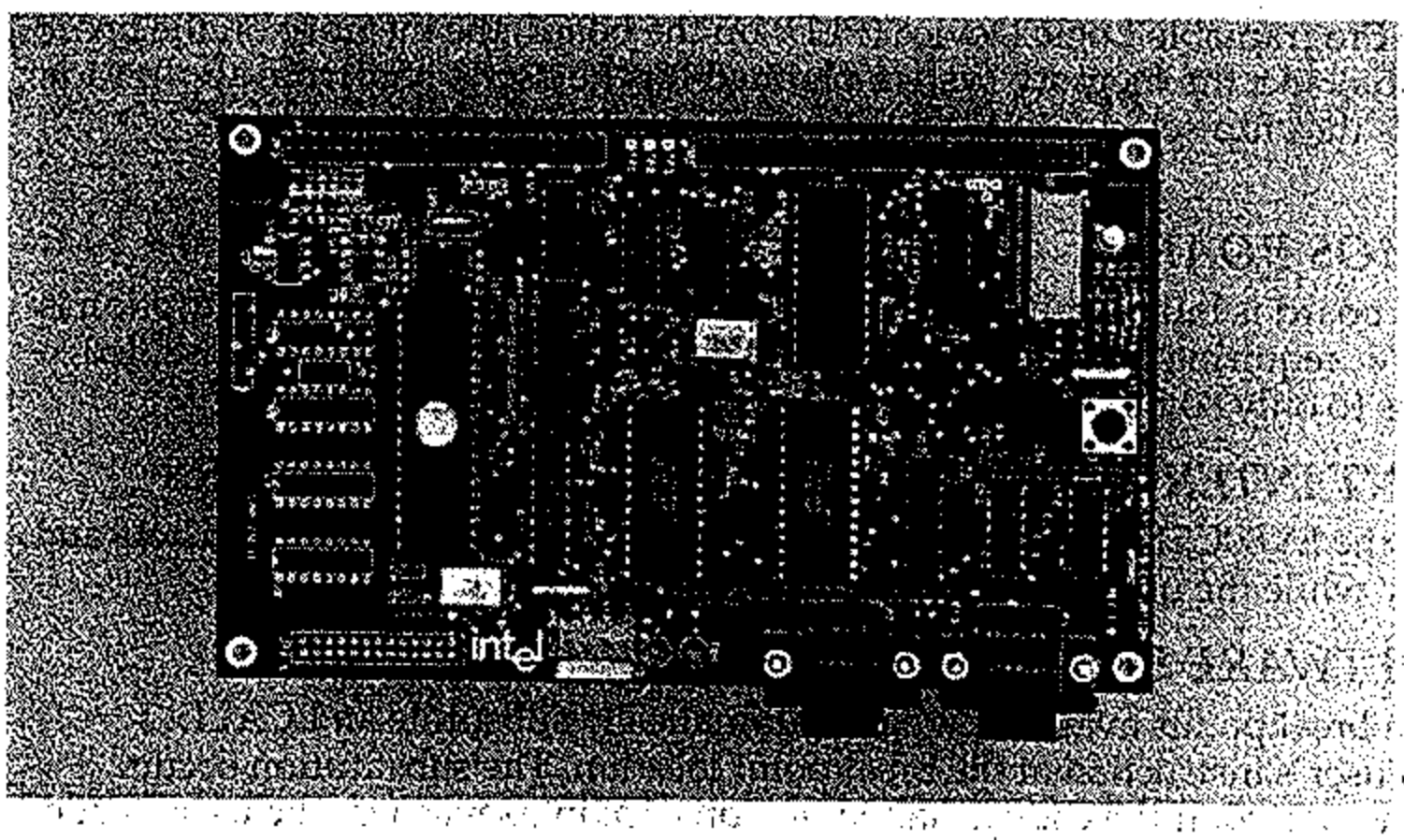
EV80C51FC EVALUATION BOARD

PRELIMINARY



LOW COST CODE EVALUATION TOOL

Intel's EV80C51FC evaluation board provides a hardware environment for code execution and software debugging at a relatively low cost. The board features the 80C51FC, single chip, CHMOS*, 8-bit microcontrollers, the newest member of the industry standard 8051 family. The board allows the user to take full advantage of the power of the 8051. The EV80C51FC provides up to 16 MHz execution of a user's code. Plus, its memory (ROMsim) can be reconfigured to match the user's planned memory system, allowing for exact analysis of code execution speeds in a particular application.

Popular features such as a single line assembler/disassembler, single-step program execution and sixteen software breakpoints are standard on the EV80C51FC. Intel provides a complete code development environment using assembly language (ASM-51) as well as Intel's high-level language PL/M-51 to accelerate development schedules.

The evaluation board is hosted on an IBM PC** or BIOS-compatible clone, already a standard development solution in most of today's engineering environments. The source code for the on-board monitor (written in ASM-51) is public domain. The program is about 3K bytes and can be easily modified to be included in the user's target hardware. In this way, the provided PC host software can be used throughout the development phase.

EV80C51FC FEATURES

- **Up to 16 MHz Execution Speed**
- **32K Bytes of ROMsim**
- **Flexible Chip-Select Controller**
- **Totally CMOS, low power board**
- **Concurrent Interrogation of Memory and Registers**
- **Sixteen Software Breakpoints**
- **Program Step Mode**
- **High-Level Language Support**
- **Single Line Assembler/Disassembler**
- **RS-232-C Communication Link**

FULL SPEED EXECUTION

The EV80C51FC executes the user's code from on-board ROMsim at up to 16 MHz. By changing crystals on the 80C51FC any slower execution speed can be evaluated. The board's host interface timing is not affected by this crystal change.

32K BYTES OF ROMSIM

The board comes with 32K bytes of SRAM to be used as ROMsim for the user's code and as data memory if needed.

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*CHMOS is a patented Intel process.
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FLEXIBLE MEMORY DECODING

By changing the Programable Logic Device (PLD) on the board, the memory on the board can be made to look like the memory system planned for the user's hardware application. The PLD controls the chip-select inputs on the board with 64 byte boundaries of resolution.

TOTALLY CMOS BOARD

The EV80C51FC board is built totally with CMOS components. Its power consumption is therefore very low, requiring 5 volts at only 225 mA. If the on board LED's are disabled, the current drops to only 80 mA. The board also requires +/- 12 volts at 10 mA.

CONCURRENT INTEROGATION OF MEMORY AND REGISTERS

The monitor for the EV80C51FC allows the user to read and modify internal registers and external memory while the user's code is running in the board.

SIXTEEN SOFTWARE BREAKPOINTS

There are sixteen breakpoints available which automatically substitute an LCALL instruction for a user's instruction at the breakpoint location. The substitution occurs when execution is started. If the code is halted or a breakpoint is reached, the user's code is restored into the ROMsim.

PROGRAM STEP MODE

The stepping mode redirects the external interrupt 0 vector for use by the monitor. All other interrupts are available to the user, and will function as normal. External interrupt 0 is returned to the user after stepping.

HIGH LEVEL LANGUAGE SUPPORT

The host software for the EV80C51FC board is able to load absolute object code generated by ASM-51, PL/M-51 or RL-51, which are available from Intel.

SINGLE LINE ASSEMBLER/DISASSEMBLER

The host has a Single Line Assembler, and a Disassembler, to simplify modification and examination of code loaded on the board.

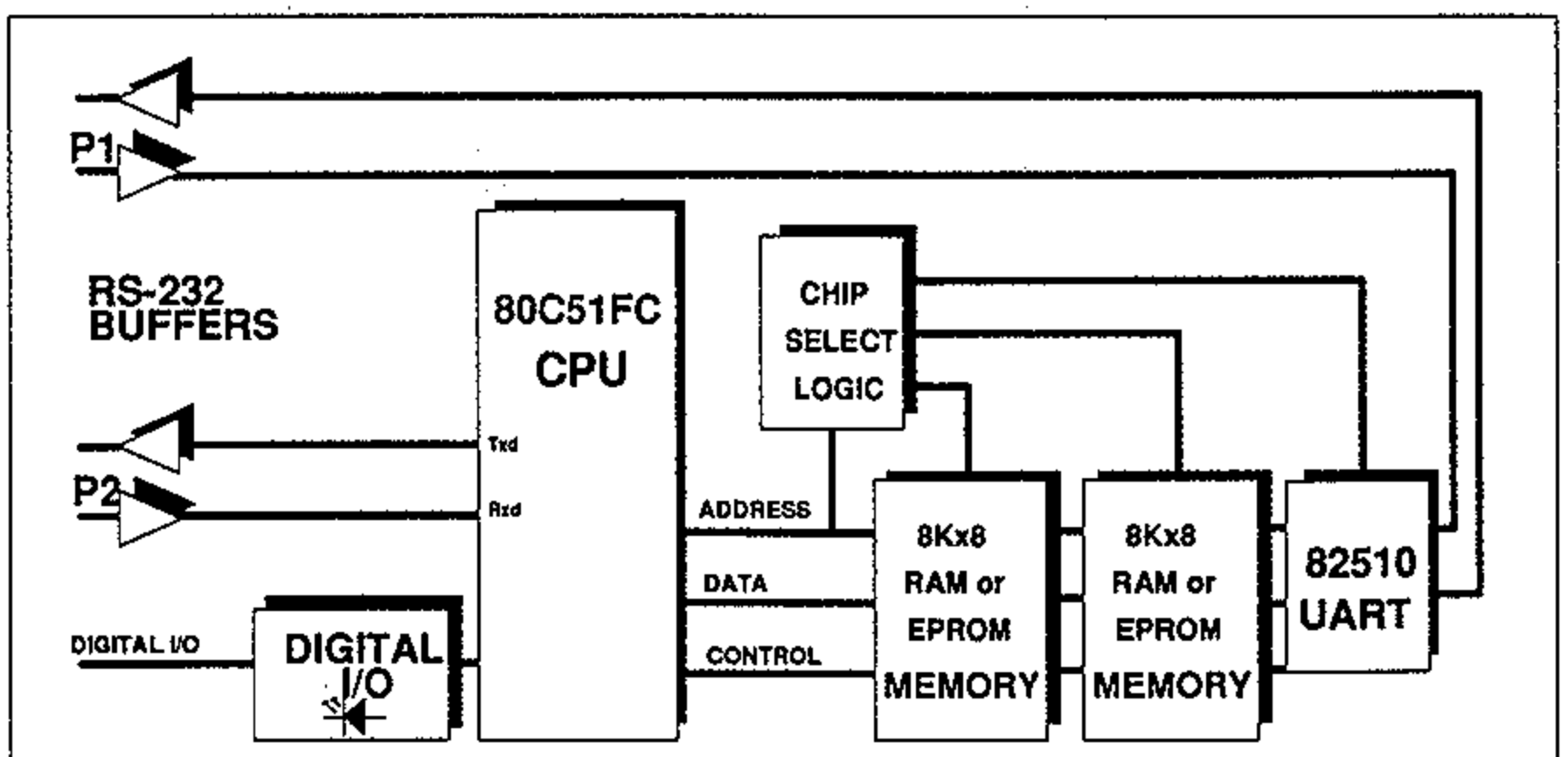
RS-232-C COMMUNICATION LINK

The EV80C51FC communicates with the host using an Intel 82510 UART provided on board. This frees the on-chip UART of the 80C51FC for the user's application.

PERSONAL COMPUTER REQUIREMENTS

The EV80C51FC Evaluation Board is hosted on an IBM PC**, XT**, AT** or BIOS compatible clone. The PC must meet the following minimum requirements:

- 512K Bytes of Memory
- One 360K Byte floppy Disk Drive
- PC DOS** 3.1 or Later
- A Serial Port (COM1 or COM2) at 9600 Baud
- ASM-51 or PL/M-51
- A text editor such as AEDIT



Block Diagram of the EV80C51FC Board